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Description

INTEGRATED CIRCUIT HAVING PAIRS OF PARALLEL COMPLEMENTARY FINFETS

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention generally relates to transistors and more particularly to the fin type transistors known as FinFETs and to forming two or more FinFETs in the space of a single conventional FinFET.

[0003] Description of the Related Art

[0004] As the need to decrease the size of transistors continues, new and smaller types of transistors are created. One recent advance in transistor technology is the introduction of fin type field effect transistors that are known as FinFETs. U.S. patent 6,413,802 to Hu et al. (hereinafter "Hu"), which is incorporated herein by reference, discloses a FinFET structure that includes a center fin that has a channel along its center and source and drains at the ends of the

fin structure. A gate conductor covers the channel portion.

[0005] While FinFETs structures reduce the size of transistor based devices, it is still important to continue to reduce the size of FinFETs transistors. The invention described below provides a method/structure which allows two or more FinFETs to be formed in the place where previously only one FinFET could be previously formed, thereby approximately doubling the density of the FinFETs.

Summary of Invention

[0006] The invention provides an integrated circuit structure that utilizes complementary fin-type field effect transistors (FinFETs). The invention has a first-type of FinFET which includes a first fin, and a second-type of FinFET which includes a second fin running parallel to the first fin. The invention also has an insulator fin positioned between the source/drain regions of the first first-type of FinFET and the second-type of FinFET. The insulator fin has approximately the same width dimensions as the first fin and the second fin, such that the spacing between the first-type of FinFET and the second-type of FinFET is approximately equal to the width of one fin. The invention also has a common gate formed over channel regions of the first-type of FinFET and the second-type of FinFET. The gate

includes a first impurity doping region adjacent the first-type of FinFET and a second impurity doping region adjacent the second-type of FinFET. The differences between the first impurity doping region and the second impurity doping region provide the gate with different work functions related to differences between the first-type of FinFET and the second-type of FinFET. The first fin and the second fin have approximately the same width.

[0007] The invention also provides a method of forming pairs of complementary parallel fin-type field effect transistors (FinFETs). The method forms a semiconductor layer on a substrate. Next, the method forms a mandrel structure that has substantially vertical sidewalls on the semiconductor layer. The method forms a series of three layers of spacers on the sidewalls of the mandrel structure. The method removes the mandrel structure and the middle spacer of the spacers, such that an inner spacer and an outer spacer remain extending from the semiconductor layer. The method then patterns the semiconductor layer, using the inner spacer and the outer spacer as masks such that regions protected by the inner spacer and the outer spacer remain as a first fin and a second fin extending from the substrate. The method dopes channel re-

gions in the first fin and the second fin differently from one another using angled implantations.

[0008] The method also forms a gate conductor over a central region of the first fin and the second fin. The method dopes portions of the first fin and the second fin not protected by the gate conductor to form source and drain regions in the first fin and the second fin. The method then insulates the source/drain regions of the first fin from source/drain regions of the second fin.

[0009] The doping of the channel regions includes doping the first fin with a first channel doping species from an angle that is substantially perpendicular to the first fin such that the first fin protects the second fin from receiving the first channel doping species. The process forms the semiconductor layer which provides a second channel doping species within the semiconductor layer. The doping of the channel regions also dopes the second fin with a second channel doping species from an angle that is substantially perpendicular to the second fin such that the second fin protects the first fin from receiving the second channel doping species.

[0010] The method also includes a process that forms the series of three layers of spacers. The method forms the inner

spacer along a sidewall of the mandrel structure. The method also forms the middle spacer on the inner spacer and the outer spacer on the middle spacer. The process of doping the source and drain regions implants different dopants at different angles into source and drain regions of the first fin and the second fin.

[0011] The mandrel structure includes two parallel sidewalls and simultaneously forms pairs of spacer structures adjacent each of the sidewalls. The mandrel structure and the middle spacer comprise similar material, such that the removing process removes the mandrel and the middle spacer in a single process. The process of insulating the source and drain regions deposits dielectric materials over the first fin and the second fin and then removes the dielectric material from all areas except between the source and drain regions of the first fin and the second fin.

[0012] The invention also provides a method of forming parallel fin structures on a substrate that forms a mandrel structure that has substantially vertical sidewalls on the semiconductor layer. The method forms a series of three layers of spacers on the sidewalls of the mandrel structure, and then removes the mandrel structure and the middle spacer of the spacers, such that an inner spacer and an

outer spacer remain extending from the substrate. The inner spacer and the outer spacer can include conductors, semiconductors; and mask elements, that are used to pattern features into the substrate.

[0013] The method also includes a process that forms a series of three layers of spacers. The method forms the inner spacer along a sidewall of the mandrel structure. The method also forms the middle spacer on the inner spacer, and the outer spacer on the middle spacer. The spacers all have approximately the same width, such that the inner spacer is separated from the outer spacer by the width of one spacer.

[0014] The invention also provides a method of forming parallel structures on a substrate. The method forms a layer of material on the substrate. The method then forms a mandrel structure that has substantially vertical sidewalls on the layer of material. The method forms a series of three or more layers of spacers on the sidewalls of the mandrel structure. The method then removes the mandrel structure and alternate layers of the spacers, such that evenly separated spacer layers remain extending from the underlying material. The method patterns the layer of material using the inner spacer and the outer spacer as masks,

such that regions protected by the evenly separated spacer layers remain as multiple fins extending from the substrate.

Brief Description of Drawings

[0015] The invention will be better understood from the following detailed description of preferred embodiments of the invention with reference to the drawings, in which:

[0016] Figure 1 is a schematic diagram of a dual-density structure according to the invention;

[0017] Figure 2 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0018] Figure 3 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0019] Figure 4 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0020] Figure 5 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0021] Figure 6 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0022] Figure 7 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0023] Figure 8 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0024] Figure 9 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0025] Figure 10 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0026] Figure 11 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0027] Figure 12 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0028] Figure 13 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0029] Figure 14 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0030] Figure 15 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0031] Figure 16 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0032] Figure 17 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0033] Figure 18 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0034] Figure 19 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0035] Figure 20 is a schematic diagram of a partially completed

dual-density FinFET structure according to the invention;

[0036] Figure 21 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0037] Figure 22 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention;

[0038] Figure 23 is a schematic diagram of a partially completed dual-density FinFET structure according to the invention; and

[0039] Figure 24 is a schematic diagram of a cross-coupled FinFET structure according to the invention.

Detailed Description

[0040] As mentioned above, the invention allows two or more FinFETs to be formed in the space where previously only one FinFET could be formed, thereby approximately doubling (quadrupling, etc.) the density of the FinFETs. The structure utilized by the invention is shown in Figure 1 which shows a top view. Figure 1 illustrates four fins 100, 102 that define four separate transistors. More specifically, the fins 100 form P-type field effect transistors (PFETs) and the fins 102 form N-type field effect transistors (NFETs). An insulator 104 separates the two fins. The gates which surround the channel regions of the fins are shown as items 106. The gate contacts are shown as

items 112, while the contacts for the source and drain of the various transistors shown are labeled item 108. Item 110 represents an insulator region that can comprise the isolation region that separates the various transistors. While Figure 1 illustrates complementary N-type and P-type transistors, one ordinarily skilled in the art would understand after reading this disclosure that the structure is not limited to complementary type transistors and could comprise any form of transistor based structure. While the description focuses on an exemplar two-FinFET structure, one ordinarily skilled in the art would understand after reading this disclosure that the structure is not limited to pairs and multiple FinFETs could be formed.

[0041] Figures 2-23 illustrate various stages of processing when manufacturing the device. Figure 2 illustrates a cross-sectional diagram of a laminated structure that includes a substrate 20, oxide layer 21, silicon layer 22, and a masking layer 23 (such as an oxide or other masking material). The substrate 20, oxide layer, 21, and silicon layer 22 comprise a silicon-over-insulator (SOI) structure that isolates the silicon 22 from the underlying substrate 20 which improves the transistors performance dramatically.

[0042] The masking layer 23 is patterned to form a polygon

structure 23 (stripe, mesa, mandrel, rectangular box, etc.) 23 as shown in top-view in Figure 3 and cross-sectional view in Figure 4. Then, as shown in top and cross-sectional views in Figures 5 and 6, a series of sidewall spacers 60-62 are formed around the mesa 23. The sidewall spacers 60-62 are formed by depositing a material and then performing a selective anisotropic etching process that removes material from horizontal surfaces at substantially higher rates than it removes material from vertical surfaces. This process leaves the deposited material only along the sidewalls of the existing structures. This process of forming sidewall spacers is repeated to form the three different sidewall spacers 60-62 shown in Figures 5 and 6. The inner and outer sidewall spacers 60, 62 are formed of a hard material (such Si3N4 or other hard masking material) while the middle spacer 61 is formed of a sacrificial material such as an oxide or other material so that it can be selectively etched with respect to the inner and outer spacers 60, 62.

[0043] One advantage of using spacer technology is that spacers can have sizes that are smaller than the minimum-sized lithographic feature that can be formed using state of the art lithographic techniques. For example, if the width of

the mesa 23 has the smallest width possible, as limited by the then current state of art lithographic techniques, the spacers formed on the sides of the mesa 23 will be sub-lithographic in size (smaller than the smallest possible lithographic size). In addition, the spacers are self aligned with the mesa structure 23 and each other, which eliminates the need to align the spacers.

[0044] Next, as shown in the top and cross-sectional views in Figures 7 and 8, the sacrificial spacer 61 and the mandrel 23 are removed using a selective etching process that removes the mesa 23 and spacer 61, yet does not substantially affect the harder structures such as the silicon 22, and the inner and outer spacers 60, 62. While some specific materials are mentioned in this disclosure, virtually any materials could be used for the structures described herein so long as the mesa 23 and the middle spacer 61 can be selectively removed with respect to the inner and outer spacers 60, 62. Preferably, the middle spacer 61 and the mesa 23 are formed of the same (or very similar material), which would permit simultaneous removal of both structures.

[0045] In Figure 9, the silicon 22 is patterned in an etching process using the spacers 60, 62 as masks. In addition, be-

fore or after this step, the spacers can be planarized to remove any rounding on the upper surfaces. While the following description utilizes the patterned structures to form FinFETs, one ordinarily skilled in the art would understand (in light of this disclosure) that the structures themselves could be used as conductors, semiconductors, insulators, structural supports, masks, etc. Therefore, while the following description centers on transistors, the invention is not limited thereto. Figure 9 also illustrates an ion implantation process that dopes the channel regions of the fins. In this example, the ion implantation is N-type and P-type. However, many other types of transistors could be formed, dependent upon the specific design requirements, and the invention is not limited to the specific types of transistors used in these exemplary embodiments. Further, in this example, the ion implantations are angled so that the silicon portions below spacers 60 only receive the first type of implant (P-type) while the silicon portions below spacers 62 only receive the second type of implant (N-type). By using an angled implantation process, the spacer and fin that is closer to the perpendicular direction from which the implant is directed shields the adjacent fin that is further from the perpendicular direc-

tion from which the implant is directed.

[0046] Next, a gate 100 is patterned over each of the pairs of fins, as shown in Figure 10. As is common with FinFET technology, the gate 100 surrounds both sides and the top of the fin along the center portion of the fin (the channel region of the fin). The region shown by line A-A in Figure 10 is shown in cross-sectional view in Figure 11 and the region shown by line B-B in Figure 10 is shown cross-sectional view in Figure 12. In order to provide different work functions for the portion of the gate which is above the N-type doped silicon verses the P-type doped silicon, the gate can undergo different types of angled implants (from different angles that are all perpendicular to the longitudinal direction of the parallel fins) as was done to dope the channel regions 22, above. Alternatively, the gate material itself can be pre-doped (include some level of impurity prior to being deposited) and then an additional angled doping implant can be performed on one side of the gate conductor to perform a different implantation into one side of the gate structure 100 to change the work function of that side of the gate conductor. Once again, by performing an angled implant(s), the side of the gate conductor that is away from the direction from which

the angled implant is directed will be shielded from the implant, thereby allowing different portions of the gate conductors to receive different work function implants. After this, the source and drain regions of the fins (the regions not covered by the gate conductors) 130 receive the source and drain dopants as shown in Figure 13. If different dopants are used for the source and drain, the individual fins can be doped selectively, again using angled implants of different impurities from different perpendicular angles as discussed above.

[0047] Figures 14 and 15 illustrate a conformal dielectric layer 140 (such as a nitride, etc.) deposited over the entire structure. Figure 14 is a cross-sectional view along line A-A while Figure 15 is a cross-sectional view along line B-B. Figures 16 and 17 illustrate that the dielectric 140 is next removed in, for example, a selective etching process from all areas except between the source and drain regions 130 of the fins. Indeed, as shown in Figure 17, the dielectric 140 is even recessed below the top of the fin. Figure 17 is a cross-sectional view along line A-A of the top view shown in Figure 16. The view along line B-B would appear the same as shown and Figure 12 because, as stated above, the dielectric 140 only remains between the

source/drain regions 130.

[0048] As shown in Figure 18, which is a cross-sectional view of the source/drain regions along line A-A, the exposed silicon areas 22 are silicided forming silicide regions 181. Next, a conductor such as tungsten 180 is deposited over the entire structure. Figure 19 illustrates the tungsten 180 overlying the channel region and gates of the fins that appears along line B-B. In Figures 20 and 21, the tungsten is recessed below the top of the fins. Figure 20 is a cross-sectional view of the source/drain regions along line A-A and Figure 21 is a cross-sectional view of the gate/channel region along line B-B.

[0049] Figure 22 illustrates a cross-section sectional view of the source/drain regions along line A-A and shows the additional processing where the tungsten 180 is patterned to remove the tungsten from a region 220 between the sets of fins. Figure 23 illustrates the same patterning 220 of the tungsten 180 in the channel/gate region along line B-B. Figure 1 illustrates the additional patterning of the tungsten 180 into the various contacts 108, 112, etc., that are described above. In addition, the structure shown Figure 1 has additional dielectrics deposited in order to isolate the different structures. Various planarization pro-

cesses can be performed, as are well known to those ordinarily skilled in the art, to complete the structure.

[0050] Figure 24 is a schematic view of the inventive high-density SRAM cell structure that includes pairs of transistors 244-247 (where each box represents one pair of parallel complementary transistors) crossed coupled with wiring patterns 248. Item 241 represents the ground line and item 242 represents the voltage line. Item 249 represents the bitline contacts. Item 243 represents the wordline acting as gate of access transistors. While Figure 24 shows one exemplary circuit using the inventive transistors, one ordinarily skilled in the art would understand (in light of this disclosure) that many additional and different FinFET based structures can be created with the invention.

[0051] As described above, the inventive process produces a structure that almost doubles the density of FinFET devices. The invention utilizes spacer technology to form the fins, which allows the fins of different transistors to be formed much closer together (only separated by one spacer width) and allows the fins to be sub-lithographic in size. The invention also provides for angled ion implants, which allows one fin to shield the other fin (in each set of fins) to permit the fins to be selectively doped differently.

Therefore, the invention easily produces complementary transistors. The complementary transistors share a gate and can be contacted individually allowing the formation of integrated circuits in a smaller area. The invention also provides a method to form pairs of fins, that could be formed into transistors, or used as wires or resistors to contact each fin independently.

[0052] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.